REMARKS

Claims 1-17 are pending in the application. Applicants amend claims 1, 7-8, 12, and 14-15 for further clarification. No new matter has been added.

Claims 7-8 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

Applicants amend claims 7-8 to correct the antecedent basis issue raised by the Examiner, and respectfully request that the Examiner withdraw the rejection.

Claims 1-5 and 16-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,046,629 to Wu et al. in view of U.S. Patent No. 6,633,567 to Brown; claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. in view of Brown, and further in view of U.S. Patent No. 6,963,575 to Sistanizadeh et al.; claims 9-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. in view of Brown, and further in view of U.S. Patent No. 6,308,218 to Vasa.; and claims 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vasa in view of Brown, and further in view of Sistanizadeh et al. Applicants amend claims 1 and 7-8 in a good faith effort to further clarify the invention as distinguished from the cited references, and respectfully traverse the rejections.

Wu et al. describe, in col. 2, lines 32-38 thereof,

> "The method comprises the steps of a) adding a control mechanism in a learning mode of the switch; b) enabling one of a plurality of ports of the switch to detect a number of learned addresses in the address table[;] c) determining whether the number of learned addresses has exceeded a predetermined maximum number of learnable address of the address table..."

Thus, Wu et al., as cited and relied upon by the Examiner, fail to disclose classifying users into a plurality of user groups, limiting and controlling a number of learned addresses in the address learning table for each of the user groups.

And Brown describes, in col. 9, lines 32-36 thereof,

> "In the example shown above there are two bits assigned to the group member number, allowing a maximum of four VIDs per FID 230a-b. However, the number of VLANs in a group identified by a FID..." (Emphasis added

That is, Brown describes constituting each VLAN group with a plurality of VLANs, and classifying VLAN groups by group number and a VLAN that belongs to a VLAN group by group member number.

The description "maximum of four VIDs per FID" in col. 9, lines 34-35 in Brown means, however, a number of VIDs (VLANs) per FID (VLAN group), and does not mean a number of learned addresses in a learning table per a VLAN or a FID.

Accordingly, Brown, as cited and relied upon by the Examiner, fails to disclose classifying users into a plurality of user groups, limiting and controlling a number of learned addresses in the address learning table for each of user groups.

In other words, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine Wu et al. and Brown, such a combination would still have failed to disclose or suggest,

> "[a] switching apparatus for learning a source address set in a packet in an address learning table and delivering a packet on the basis of an address learned in said address learning table, said switching apparatus comprising:
> an address learning unit for limiting a number of learned addresses such that a number of learned addresses in said address learning table for each of user groups which are classified into a plurality of groups based on header information set in said packet is equal to or less than an address learning upper limit value for said user group and controlling said number of learned addresses in said address learning table for each user group;

wherein said address learning upper limit value is set
for each user group," as recited in claim 1. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 1, together with claims 2-5 and 16-17 dependent therefrom, is patentable over Wu et al. and Brown, separately and in combination, for at least the above-stated reasons. The Examiner cited Sistanizadeh et al. and Vasa as further combining references to specifically address the additional features recited in claims 6 and 9-11, respectively, which also depend from claim 1. As such, further combinations with these references would still have failed to cure the above-described deficiencies of Wu et al. and Brown, even assuming, arguendo, that such further combinations would have been obvious to one skilled in the art at the time the claimed invention was made. Accordingly, Applicants respectfully submit that claims 6 and 9-11 are patentable over the cited references for at least the foregoing reasons. Claims 7-8 incorporate features that correspond to those of claim 1 cited above. And as described above, a combination of Vasa, Brown, and Sistanizadeh et al. would still have failed to disclose or suggest each and every feature of the claimed invention. Accordingly, Applicants respectfully submit that claims 7-8 are patentable over the cited references for at least the foregoing reasons.

Claims 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. in view of Vasa; and claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. in view of Vasa, and further in view of U.S. Patent Application Publication No. 2003/0031190 to Ohnishi et al. Applicants amend claim 12 in a good faith effort to further clarify the invention as distinguished from the cited references, and respectfully traverse the rejections.

Vasa describes, in col. 5, lines 62 to col. 6, lines 7 thereof,

"A memory control module 118 provides an interface
between the memory device 200 and the communication bus

> 102 and also provides an interface between the memory device 200 and a look-up control module 120. The memory device 200 includes mailboxes 202 for exchanging information between the external processor 600 and switch engine 100. In addition, the memory device includes look-up tables 204. The look-up tables 204 include entries which indicate which port of the switch engine 100 is associated with each node of the LAN and also include group addresses for multi-cast packets. The look-up tables 204 are utilized for appropriately directing among the ports 104-112 data packets received by the switch engine 100."

That is, Vasa describes look-up tables 204 for directing among ports 104-112 data packets received by the switch engine 100 provided in the memory 200.

And therefore, Vasa, as cited and relied upon by the Examiner, fails to disclose look-up table 204 using a number of learnable addresses by using memory of look-up table 204 shared with all of user groups and an individual guaranteed value set for each of the user groups which are classified into a plurality of groups based on header information set in a packet by using memory of look-up table 204 for guaranteeing an individual guaranteed value of each user group.

Vasa describes, in col. 3, line 62 to col. 4, line 2 thereof,

> "However, if the memory pointer buffer of the destination port is nearly full, the bus controller of the destination port applies a jam request signal to the communication bus. The source port receives the jam request and, in response, discards the incoming packet and also sends a jam signal over its associated segment. The jam signal causes the node (source node) which is the source of the packet to discontinue sending the packet and attempt to resend the packet after a waiting period."

And in col. 2, lines 60-63 of Vasa,

> "The memory pointer buffer stores memory pointers in a queue for transmission by the port, one memory pointer for each data packet being stored in the packet buffers of the memory."

Thus, the memory pointer buffer described in Vasa is different from the look-up tables 204, and, therefore, Vasa, as cited and relied upon by the Examiner, fails to disclose

> "limiting a number of learned addresses on the basis of a total number threshold value which is based on a number of learnable addresses by using memory of said address learning table shared with all of said user groups and an individual guaranteed value set for each of user groups which are classified into a plurality of groups based on header information set in said packet by using memory of said address learning table for guaranteeing an individual guaranteed value of each user group," as claimed.

In other words, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine Wu et al. and Vasa, such a combination would still have failed to disclose or suggest,

> "[a] switching apparatus for learning a source address set in a packet in an address learning table and delivering a packet on the basis of an address learned in said address learning table, said switching apparatus comprising:
> an address learning unit for limiting a number of learned addresses on the basis of a total number threshold value which is based on a number of learnable addresses by using memory of said address learning table shared with all of said user groups and an individual guaranteed value set for each of user groups which are classified into a plurality of groups based on header information set in said packet by using memory of said address learning table for guaranteeing an individual guaranteed value of each user group, so as not to allow increase in a number of learned addresses for a user group which number in said address learning table exceeds said individual guaranteed value when a total number of learned addresses learned in said address learning table reaches said total number threshold value and controlling said number of learned addresses in said address learning table for each user group," as recited in claim 12. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 12 is patentable over Wu et al. and Vasa, separately and in combination, for at least the above-stated reasons. The Examiner relied upon Ohnishi et al. as a combining reference to specifically address the additional features recited in claim 13, which depends from claim 12. As such, a further combination

with this reference would still have failed to cure the above-described deficiencies of Wu et al. and Vasa, even assuming, arguendo, that such a further combination would have been obvious to one skilled in the art at the time the claimed invention was made. Accordingly, Applicants respectfully submit that claim 13 is patentable over the cited references for at least the foregoing reasons.

Claims 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0123462 to Kusayanagi in view of Brown. Applicants amend claims 14-15 in a good faith effort to further clarify the invention as distinguished from the cited references, and respectfully traverse the rejection.

Corresponding to the above, the Examiner cited Kusayanagi as a principal reference that allegedly discloses a switching apparatus, and relied upon Brown as a combining reference that allegedly suggests the claimed "number of learned addresses" features, which the Examiner acknowledged was absent from the disclosure of Kusayanagi. And as discussed above, Brown, as cited and relied upon by the Examiner, fails to disclose classifying users into a plurality of user groups, limiting and controlling a number of learned addresses in the address learning table for each of user groups.

In other words, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine Kusayanagi and Brown, such a combination would still have failed to disclose or suggest,

> "[a] switching apparatus for learning a source address set in a packet in an address learning table and delivering a packet on the basis of an address learned in said address learning table, said switching apparatus comprising:
> an address learning unit for, on the basis of a total number threshold value which is based on a number of learnable addresses by using memory of said address learning table shared with all of said user groups and an individual guaranteed value set for each of user groups which are classified into a plurality of groups based on header information set in said packet by using memory of said address

> learning table for guaranteeing an individual guaranteed value of each user group, marking an address learned in said address learning table for a user group whose number of learned addresses exceeds said individual guaranteed value at a time of learning the new address, and overwriting the marked address with a new address of a user group whose number of learned addresses is less than said individual guaranteed value when a total number of currently learned addresses reaches a maximum number of addresses learnable in said address learning table and controlling said number of learned addresses in said address learning table for each user group," as recited in claim 14. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 14 is patentable over Kusayanagi and Brown, separately and in combination, for at least the above-stated reasons. Claim 15 incorporates features that correspond to those of claim 14 cited above, and is, therefore, patentable over the cited references for at least the same reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

/Dexter T. Chang/
Dexter T. Chang
Reg. No. 44,071

CUSTOMER NUMBER 026304
Telephone: (212) 940-6384
Fax: (212) 940-8986 or 8987
Docket No.: 100794-00513 (FUJM 20.762)